FIG.1

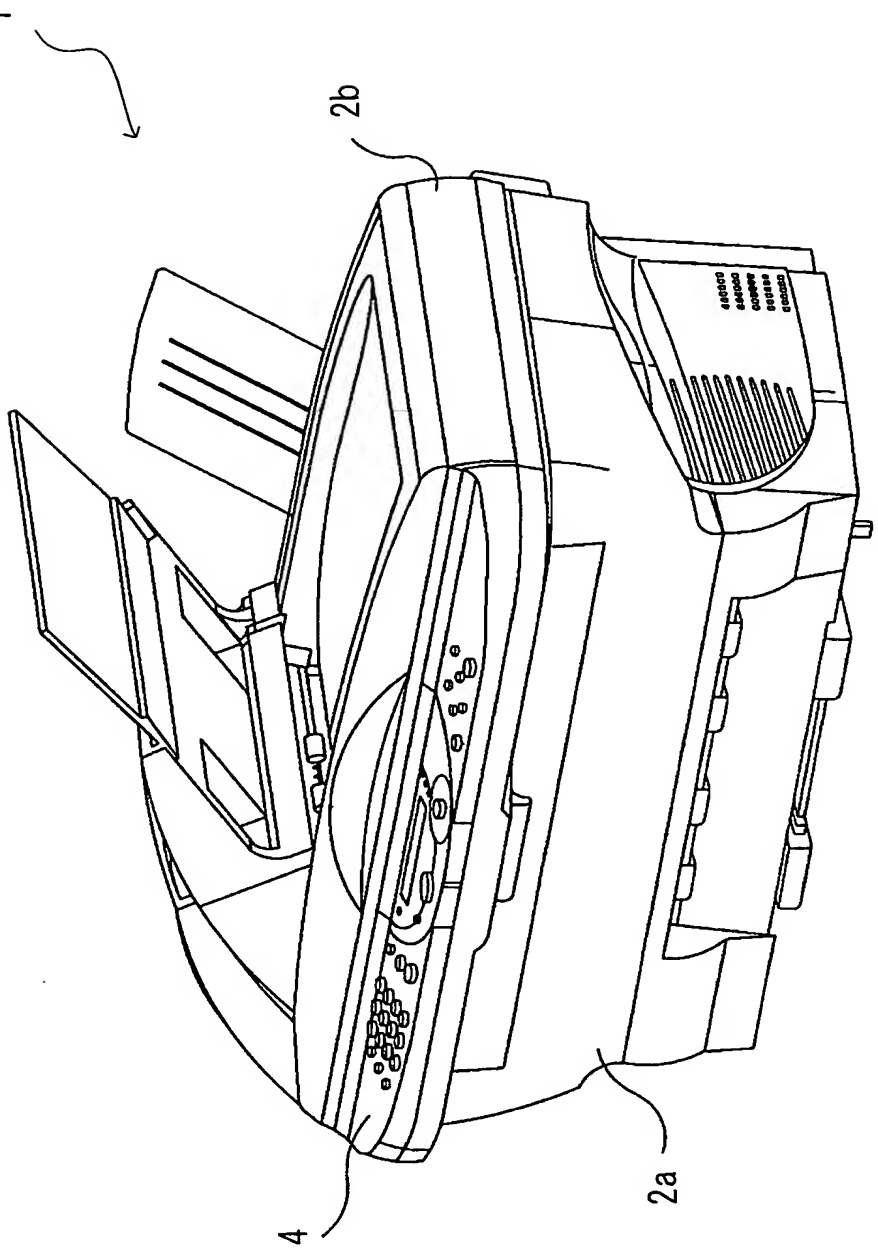


FIG.2

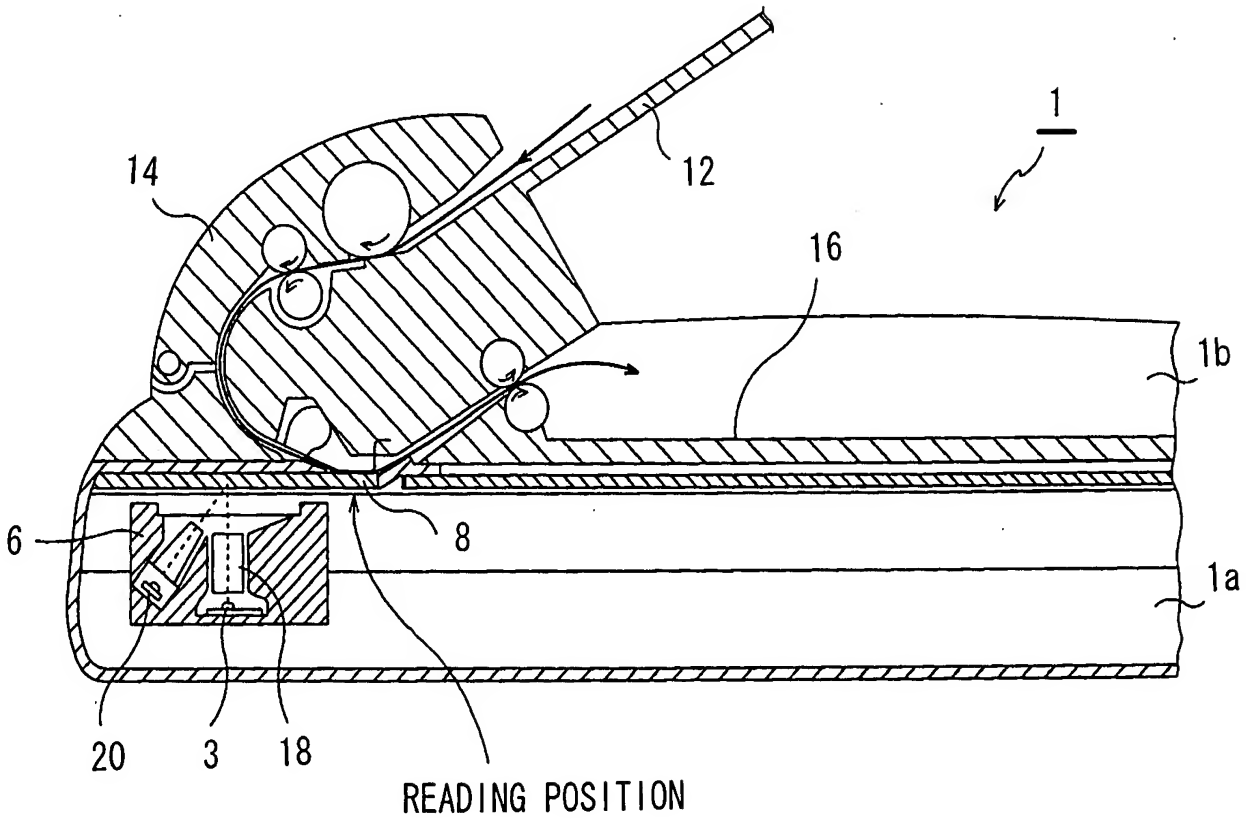


FIG.3

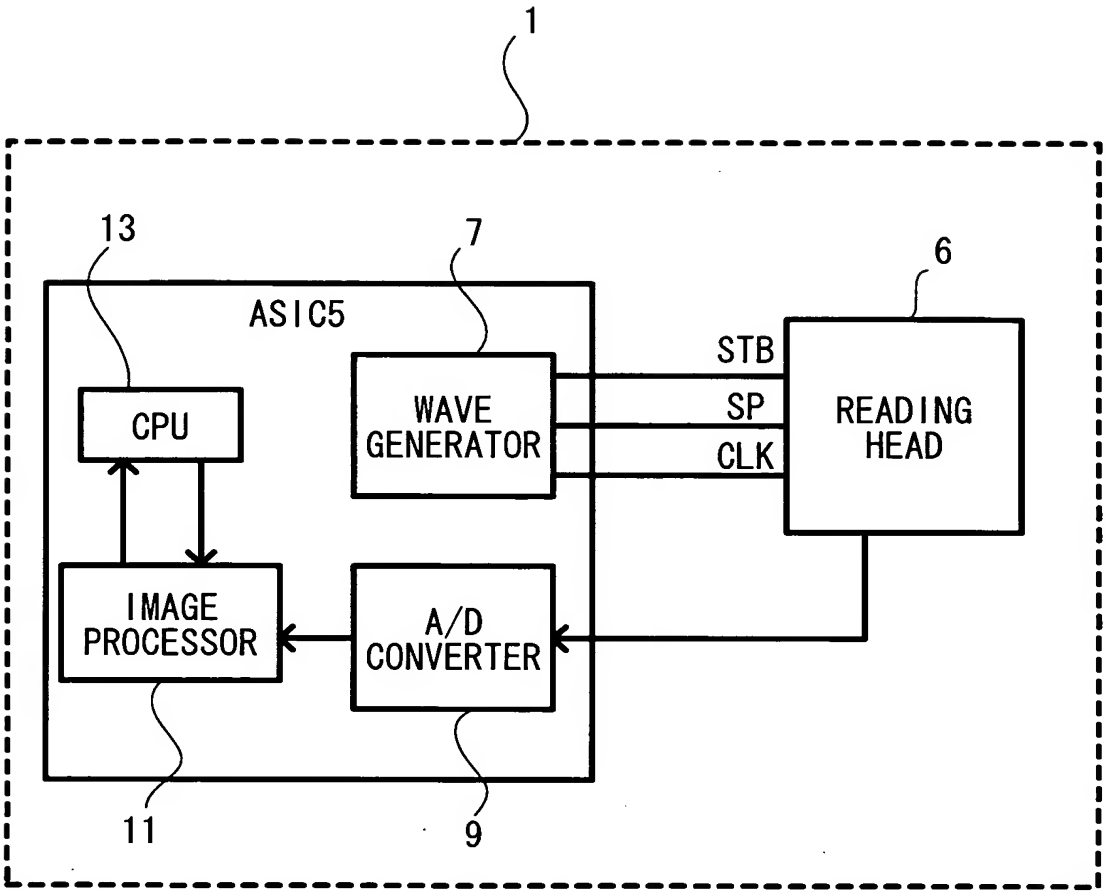

1
13
7
6
ASIC5
CPU
WAVE GENERATOR
STB
SP
CLK
READING HEAD
IMAGE PROCESSOR
A/D CONVERTER
11
9

FIG.4

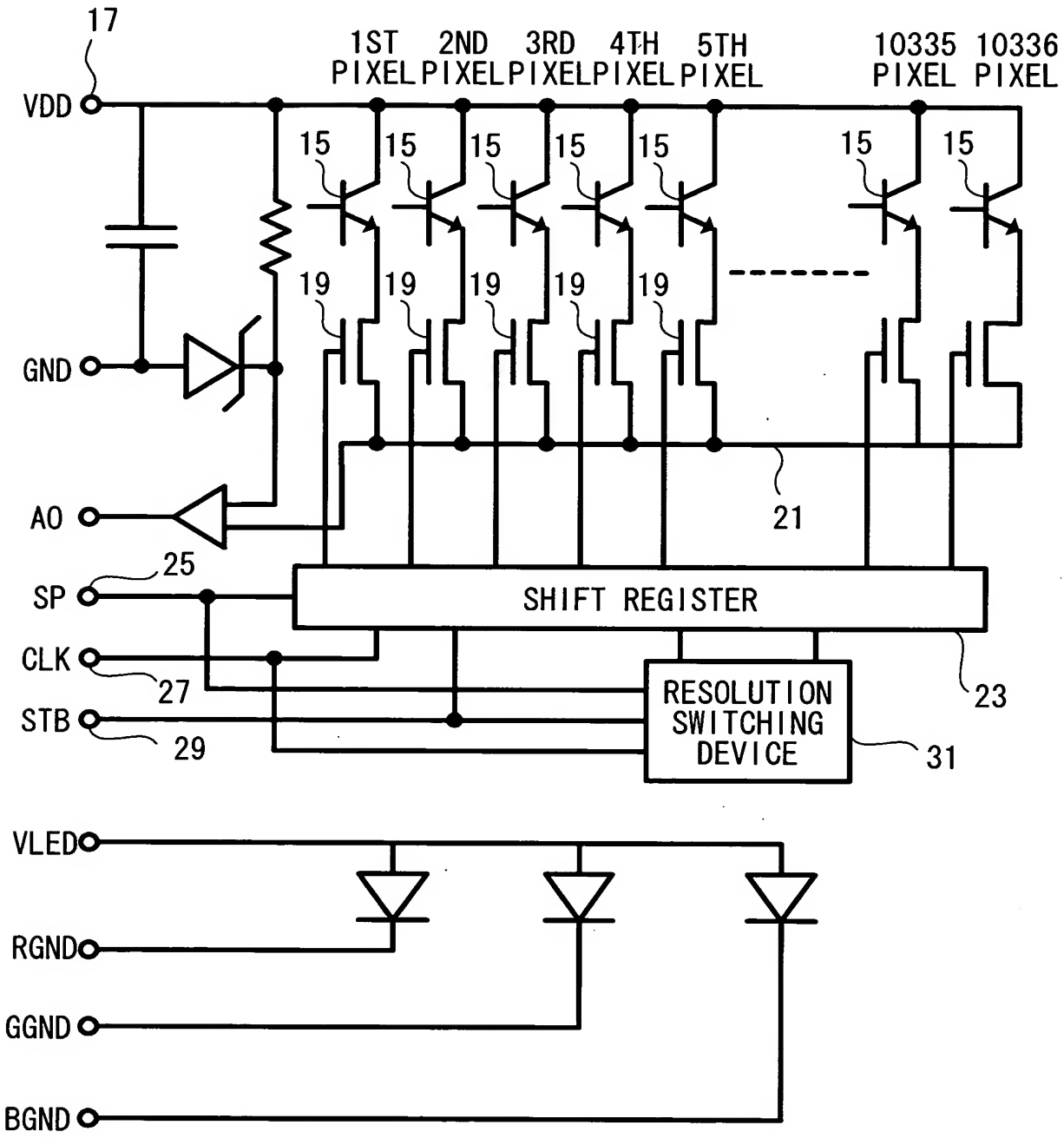

17
1ST PIXEL
2ND PIXEL
3RD PIXEL
4TH PIXEL
5TH PIXEL
10335 PIXEL
10336 PIXEL
VDD
GND
AO
SP
CLK
STB
15
19
21
23
25
27
29
31
SHIFT REGISTER
RESOLUTION SWITCHING DEVICE
VLED
RGND
GGND
BGND

FIG.5

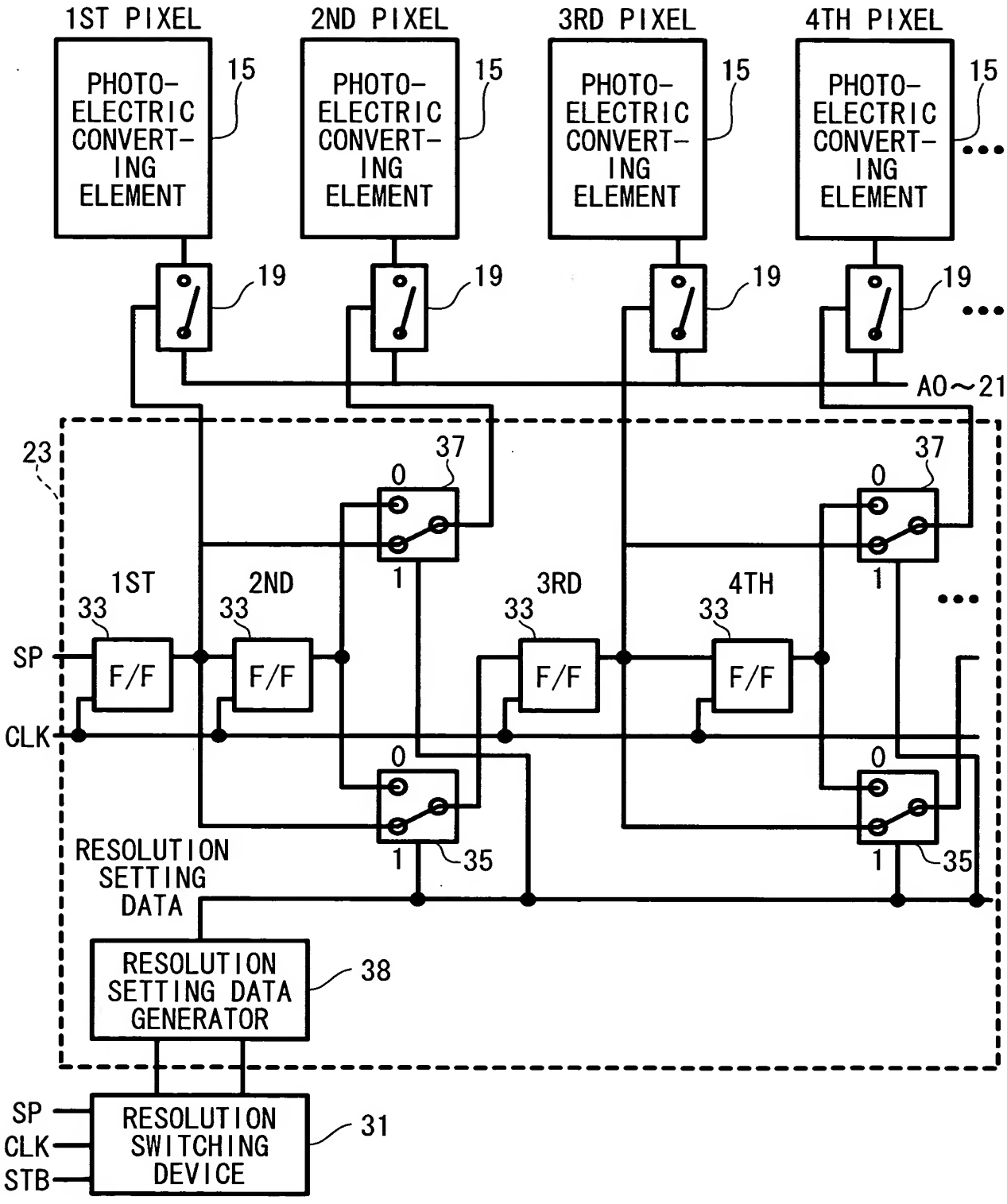

1ST PIXEL
2ND PIXEL
3RD PIXEL
4TH PIXEL
PHOTO-ELECTRIC CONVERT-ING ELEMENT
15
19
A0~21
23
37
0
1
1ST
2ND
3RD
4TH
33
SP
CLK
F/F
35
RESOLUTION SETTING DATA
RESOLUTION SETTING DATA GENERATOR
38
RESOLUTION SWITCHING DEVICE
31
STB

FIG.6

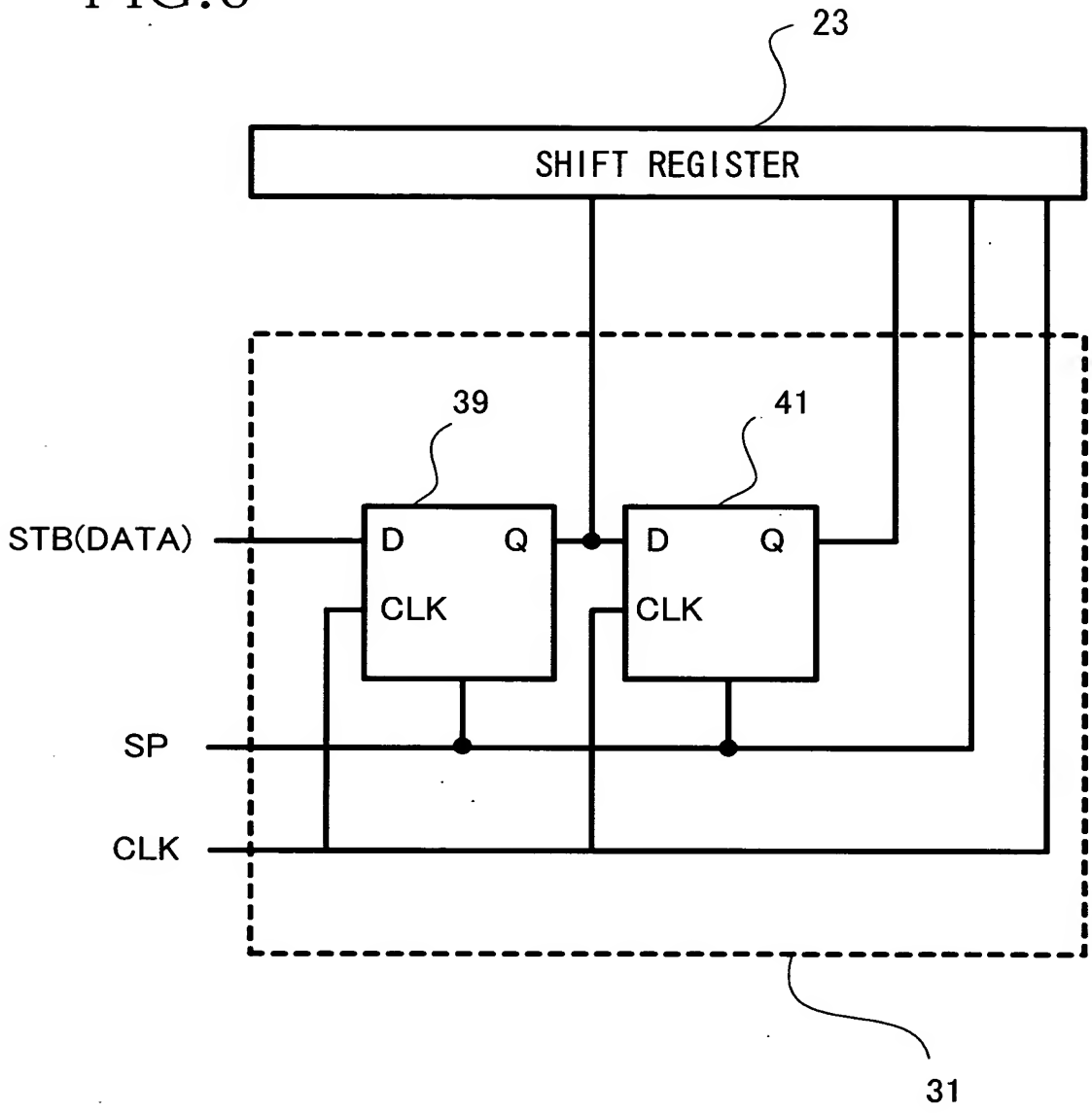


FIG.7

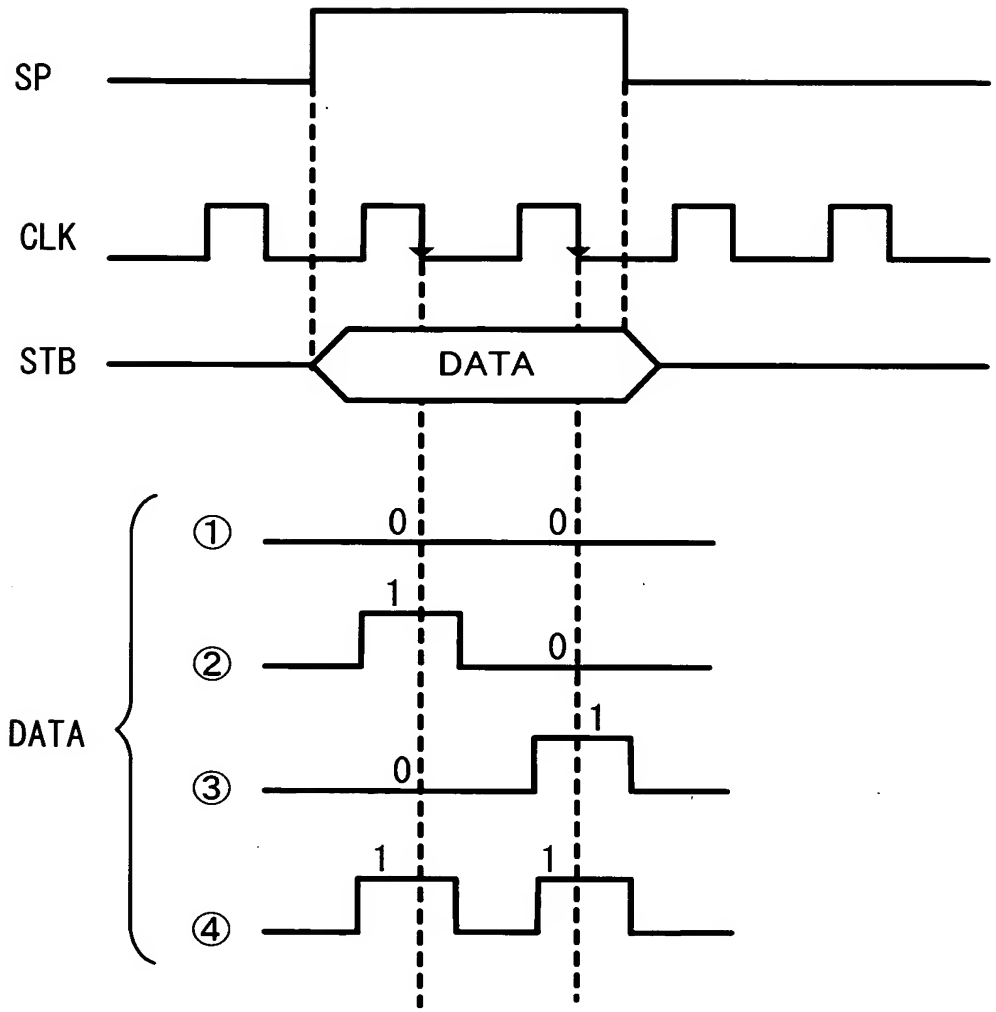


FIG.8

STB SIGNAL WAVEFORM	LATCH 39	LATCH 41	RESOLUTION SETTING DATA (dpi)
WAVEFORM 1	0	0	1200
WAVEFORM 2	1	0	600
WAVEFORM 3	0	1	400
WAVEFORM 4	1	1	300

FIG.9

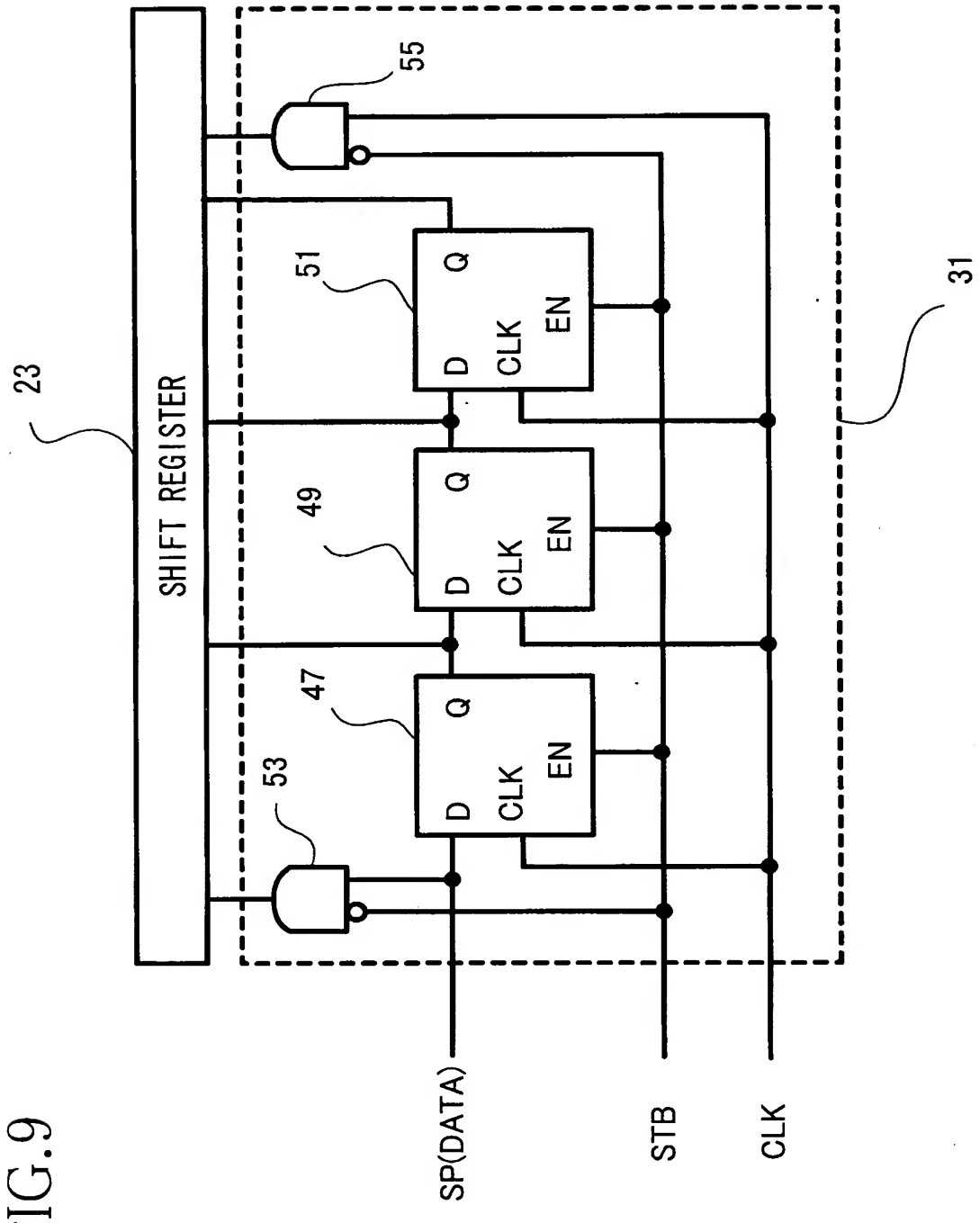


FIG.10

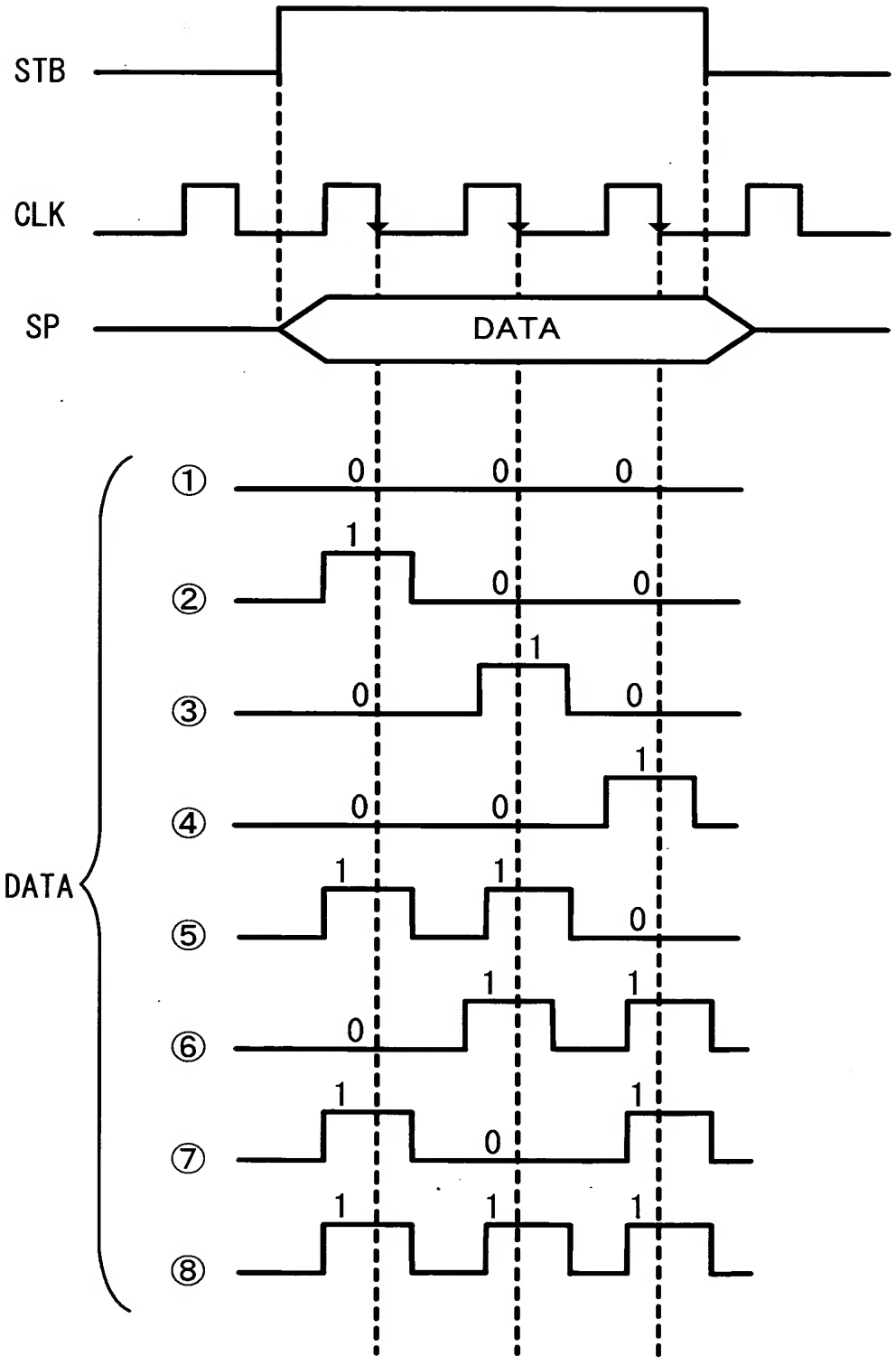
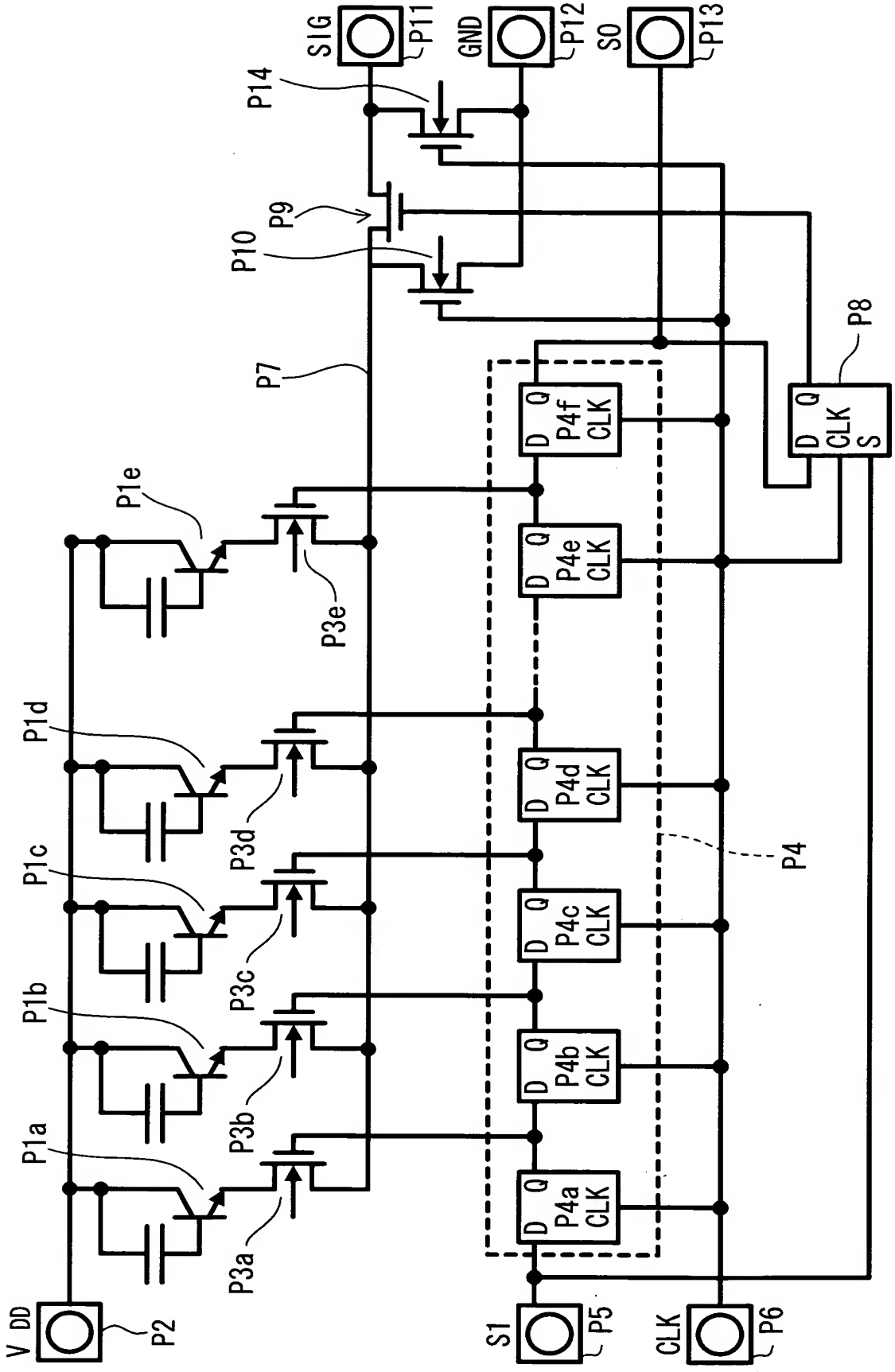


FIG.11

SP SIGNAL WAVEFORM	LATCH 49	LATCH 49	LATCH 51
WAVEFORM 1	0	0	0
WAVEFORM 2	1	0	0
WAVEFORM 3	0	1	0
WAVEFORM 4	0	0	1
WAVEFORM 5	1	1	0
WAVEFORM 6	0	1	1
WAVEFORM 7	1	0	1
WAVEFORM 8	1	1	1

FIG.12


V DD
P2
S1
P5
CLK
P6
SIG
P11
GND
P12
S0
P13
P14
P9
P10
P7
P8
P1a
P1b
P1c
P1d
P1e
P3a
P3b
P3c
P3d
P3e
P4
D Q
P4a CLK
P4b CLK
P4c CLK
P4d CLK
P4e CLK
P4f CLK
D Q
CLK S